SIMULATION OF HPF OFFLINE POWER SUPPLY FOR WIDE INPUT VOLTAGE RANGES USING IBFC

Anumol George[1], K.R. Varmah[2], Chikku Abraham[3]

Department of Electrical and Electronics Engineering
Rajagiri School of Engineering and Technology, Kakkanad
E-mail: [1]anumolge@gmail.com, [2]varmah@rajagiritech.ac.in, [3]chikkuabraham@yahoo.co.in

Abstract

Owing to the harmonic problems created by the electronic equipments in the power distribution system, the need for power factor correction is important. This paper presents a good solution for implementing a low cost, high power factor ac to dc converter for low power application with fast output regulation. A single stage converter called Integrated Buck Fly Back converter (IBFC) is used for this applications. In this both the Buck and Fly Back semi stages are operated in discontinuous conduction mode. The circuit is designed and simulated for wide input voltage, ranges from 90 – 250 Vrms, 48 V output operating at 100 kHz. The simulation is performed using PSIM© software. The closed loop control of the circuit is also analysed based on the voltage mode control strategy using a PI controller.

Index Terms Offline power supply, IBFC, high power factor, single stage converter, bulk capacitor, discontinuous conduction mode.

I. INTRODUCTION

OFFLINE power supply is a power supply in which the ac line voltage is rectified and filtered off with out using a line frequency isolation transformer. The output thus obtained is processed with a dc to dc converter that provides isolation at switching frequency. They are also known as Off Line Switchers (OLS). Despite of OLS, a simple structure consisting of bridge rectifiers and capacitor filters input current harmonics cause poor power quality of public utility network. So for improving power factor several standards [2] were introduced to impose limit over the harmonic current drawn by the equipment. This paper discuss on High Power-factor Offline power supply using Integrated Buck Flyback Converter (IBFC).

IBFC is basically derived from Flyback converter, which is good solution for output voltage regulation by maintaining High Power-factor. Integrating Power-factor correction (PFC) and dc to dc converter stages into a single stage converter (SSC) reduces the component count, cost and size of the circuit. This is particularly useful for the low-power application. Here a bulk capacitor is used for fast output voltage regulation and an input current shaper (ICS) is introduced for power-factor correction. This avoids the need for a separate power factor correction circuit. Thereby reducing the size of the circuit.

The DCM has an advantage that output power depends on the duty cycle of the control switch. In IBFC two inductors are used, Buck and Flyback. In this case the ratio between bulk capacitor voltage and peak line voltage depends only on the two inductance ratio, and independent of output power. This means that bulk capacitance voltage can be maintained for Universal input voltage range. But the value of bulk capacitor is

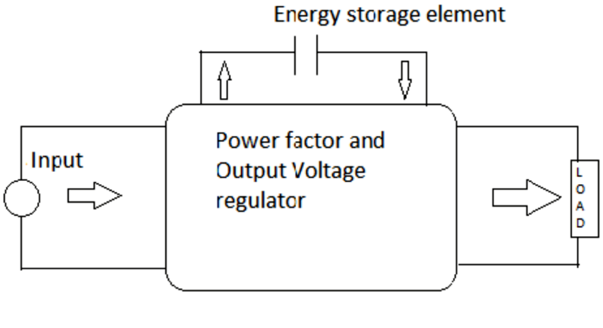

Fig. 1. Block diagram of a Single stage converter

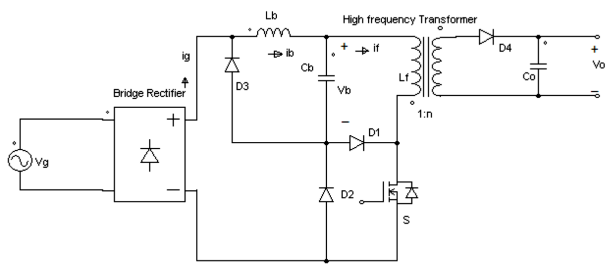

Fig. 2. Circuit diagram of High Power-factor IBFC

comparatively high. The bulk capacitor is independent on the duty cycle. Therefore changes in the duty cycle affect only output power, thus it is being regulated fast.

The important feature of IBFC that is to be highlighted in this paper is, the control switch handles lower rms current. The current through the switch is buck or flyback inductor current, whichever is higher and not the addition of two currents. Thus this paper investigates IBFC for high power factor offline application. An universal input ranging from 90 – 250 Vrms, for an output of 48 Volt, 100 Watt ac to dc converter which is operating at switching frequency 100 KHZ is designed and simulated using Software PSIM©. The simulation results shows that the power factor is maintained high at all the input voltages as specified above and output voltage is regulated fast. When load is increased from 10 – 500 ohms it is observed that the ripple in regulated output is low and it is high when load decreases.

II. OPERATIONAL PRINCIPLES OF IBFC

The Fig. 1. illustrates the basic model of an IBFC for high power factor applications. In this both buck and flyback converters are operating in discontinuous conduction mode.

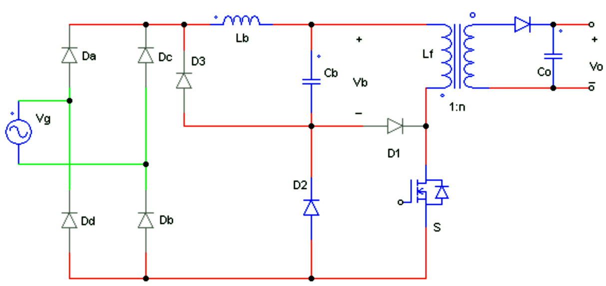

Fig. 3. IBFC when Vg < Vb

Let us consider the case when IBFC is operated during line half cycle and when instantaneous line voltage is lower than the bulk capacitor voltage. In this case the bridge diodes Da, Db, Dc, and Dd are reverse biased and remain open. Thus the buck inductor is not conducting during this interval. Also diode D1 and D3 remains open. During this time interval only the fly back converter is operating from the bulk capacitor voltage, through switch S and diodes D2 and D4 as shown in Fig. 3. This is the offline operation of IBFC.

Now consider the case when instantaneous line voltage is higher than the bulk capacitor voltage. In this interval both buck and fly back inductors conduct through the switch S, and diodes D3 and D4 remain open while others conduct as shown in Fig. 4. Also consider the case when the switch S is off at the same condition mentioned above, so that diodes D1 and D2 are not conducting while others conduct as shown in Fig. 5. It is to be noted that the output capacitor supplies the load during this period as same as the working of a simple flyback converter.

While discussing about the operational principle of IBFC there arises a question, how the first inductor works for buck converter? The answer for the question is, the bridge diode which is placed at the input side behaves as the switch and D2 behaves like a freewheeling diode. Both these components make the operation the same as working of a Buck converter. It is also to be noted that the bulk capacitor is operated in line frequency, 50 Hz and the output capacitor is operated at switching frequency, that is 100 kHz.

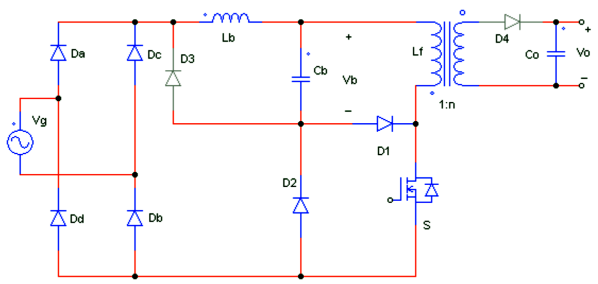

Fig. 4. IBFC when Vg > Vb and switch S ON

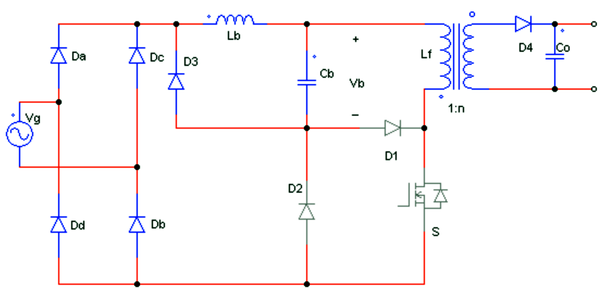

Fig. 5. IBFC when Vg > Vb and switch S OFF

III. DESIGN OF HPF IBFC

Before doing the design it is essential to know how the power factor is maintained high. For that, analysis is essential [1] and the whole design is based on it. The circuit is designed with Universal input ranging from 90 – 250 Vrms, 48 V output, 100 W ac to dc converter operating at switching frequency of 100 kHz.

In order to get a satisfactory power factor as per the standards, the conduction angle required is 105° [3] as shown in Fig. 6. The required conduction angle can be obtained from the equation $\theta = \pi - 2\sin^{-1} m$. Therefore the required voltage ratio m (V_b/V_g) for the desired conduction angle is given by

$$m = \sin\frac{(\pi - \theta)}{2} \quad (1)$$

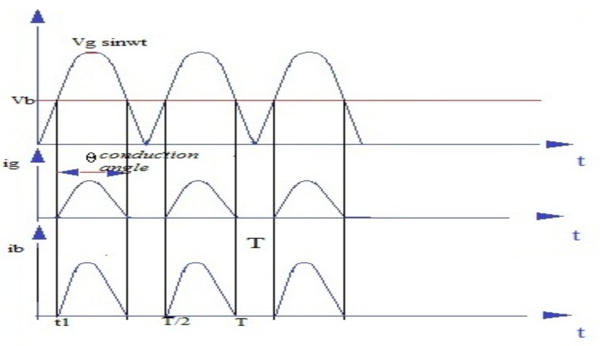

Fig. 6. Input voltage and current wave form in IBFC

Thus the voltage ratio, m is calculated as 0.6 for $\theta = 105°$. For m = 0.6 the maximum bulk capacitor voltage obtained at maximum line voltage of $250V_{rms}$is $212.13V_{rms}$ from the relation Vb/Vg = 0.6. From [1] maximum duty cycle is given by the voltage ratio m. The buck converter duty ratio is Vo/Vin, here Vo is Vb and Vin is Vg.

$$D_{buck\_}max = m \quad (2)$$

The duty ratio of buck converter is same as the voltage ratio. Flyback converter is basically buck boost converter whose duty ratio is given by Vo/Vin=D/1-D. Here Vin is Vg and Vo is Vo *i.e.* voltage across the output capacitor.

$$D_{buck\_}max = \frac{VO}{nmVg + VO} \quad (3)$$

Where n is the turn's ratio of the flyback inductor. For maximum duty cycle the line voltage should be minimum, i.e. line voltage is 90 V_{rms}. So for D = 0.6, Vb minimum obtained is 76.3 V_{rms}. Substituting this in equation (3) we get n = 0.4. The flyback inductance can be obtained from the assumption that the power delivered to the load is equal to the input power of the of the flyback semistage. This is given by

$$P_o = \frac{Vb^2}{Rf} = \frac{Vb^2}{2Lf}\frac{D^2}{Fs} \quad (4)$$

$$D = \frac{1}{Vb}\sqrt{2PoLfFs} \quad (5)$$

Where Po is the output power, Lf is the flyback inductance and Fs is the switching frequency. Substituting we get Lb = 105 μ H. With duty cycle 0.6 the inductance ratio is 0.4 and Lb thus obtained is 42 μH.

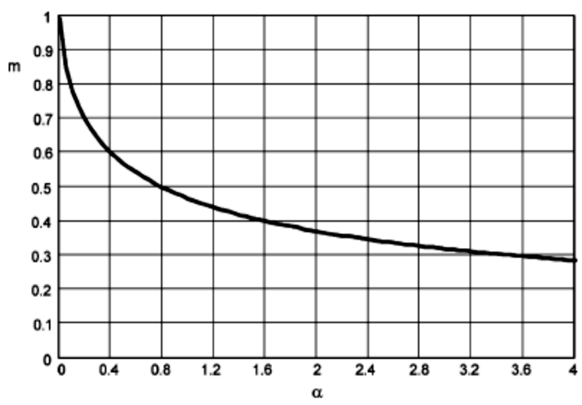

Fig. 7. Voltage ratio m as a function of inductance ratio [1]

Finally the design of bulk capacitance with the highest voltage ripple is being discussed. The highest voltage ripple occurs when the input voltage decreases. The ripple factor for m = 0.6, is 1.23 [1]. So we assume that the maximum ripple is 20% at 90 V.

$$\frac{\Delta Vb}{Vb} = \frac{v}{2\omega\, Cb\, Rb} \quad (6)$$

Thus the bulk capacitance Cb is obtained as 420 μ F.

IV. SIMULATION

The simulation is performed using PSIM© software. The simulated circuit is given in the Fig. 8. It is observed that the power factor is maintained in the range 0.92 - 0.98 as the input voltage increases from 90V_{rms} to 250 V_{rms}. In terms of peak voltage, the input voltage ranges from 127 V to 354 V. Using bulk capacitor a regulated output of 48 V is obtained at a faster rate. The simulation is also performed in different input voltage ranges. The closed loop control circuit using PI controller is done for simulation, to get good output voltage regulation maintaining high power factor.

The circuit can be explained with the initial stage rectification using diode bridge rectifier, and secondary state output regulation and power factor correction using flyback and buck converters respectively. The closed loop simulation of the circuit is performed using a voltage mode control strategy.

A. Voltage Mode Controller

As shown in Fig. 9, in the voltage mode control, the output voltage across the load is sensed and compared with the desired output voltage using an error amplifier.

The control voltage thus produced is compared with the sawtooth of comparable magnitude and the

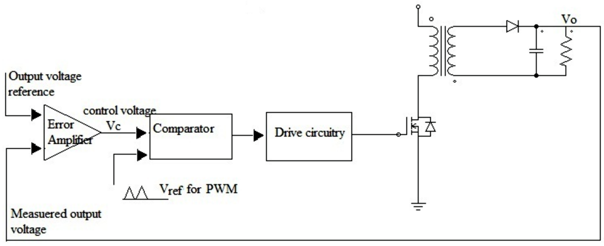

Fig. 9. Voltage mode control scheme

switching signal for the circuit is produced. There is another mode of control which is known as current mode control. In this, the current is sensed instead of sensing the voltage. ICs in UC3844 series can perform the current mode control effectively.

In the simulation circuit shown in Fig. 6. the output voltage is measured using voltage sensor which has got a gain that can be adjusted. The voltage thus obtained is compared with desired output voltage. The error signal is then passed through a PI controller for correction and then PWM signal is generated using its

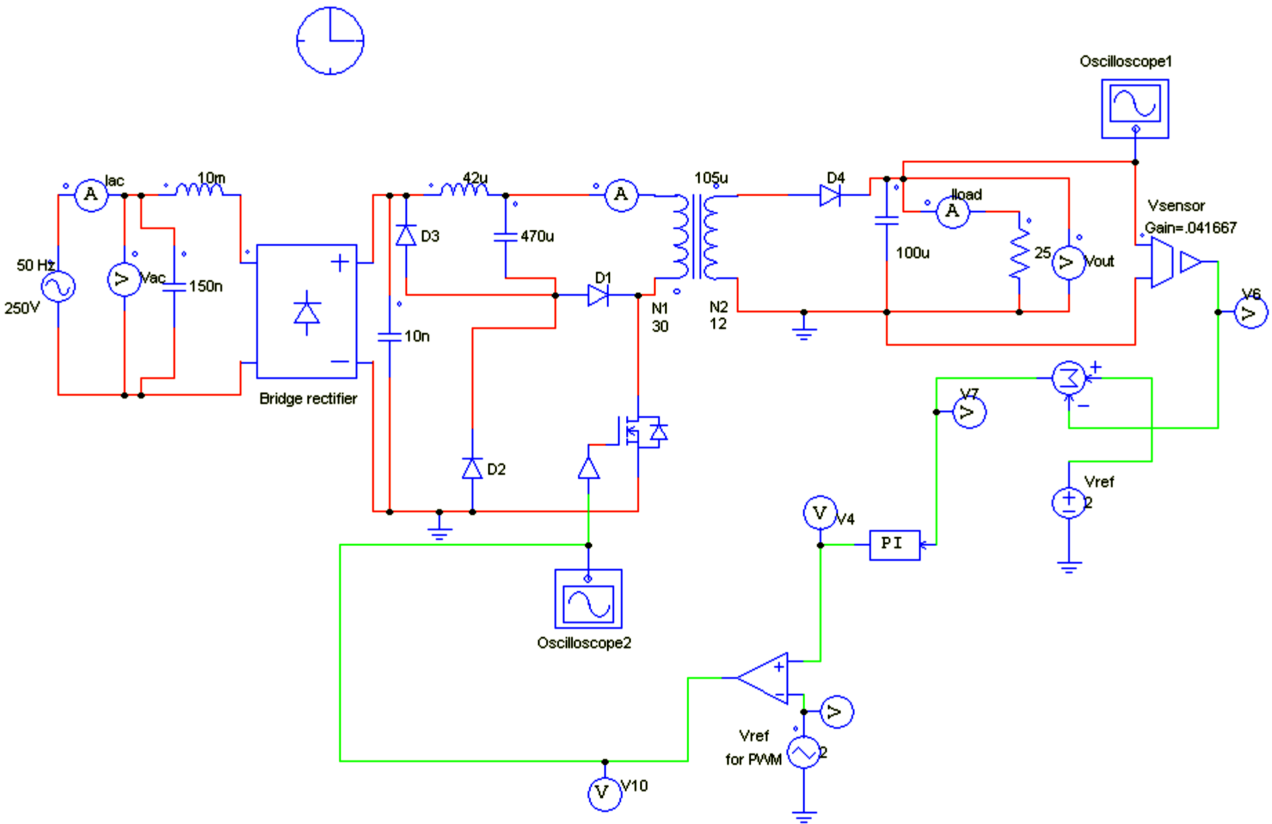

Fig. 8. Schematic diagram simulated using PSIM

output and triangular signal operating at a switching frequency of 100 kHz. For the practical implementation. the control circuit can be implemented using an ARM processer which is 32 bit, operating very fast at 3.3V. The characteristic feature of ARM processor is their low electric power consumption which makes them particularly suitable for use in portable devices.

V. SIMULATION RESULTS

The output voltage when input is 250 V peak is shown in Fig. 10. The average output voltage from the simulation tool is 46 V. From the figure it is very clear that the output voltage regulation takes fast before 0.05 s. The Fig. 11. shows the input current wave form. The peak current is about 2 A. The Fig. 12. shows the input current and voltage waveforms together. The PSIM simulation tool can measure the power factor directly from the two input waveforms. It is observed that the power factor is maintained high throughout the input range and it goes on increasing as the input voltage is increased. The Fig. 13. shows the load current waveform, the average value is maintained at 1.8 A.

The Fig. 14. and Fig. 15. shows the variation of duty cycle at the initial and steady states. The variation in the on and off time can be clearly observed. PSIM© have another option for viewing the output through oscilloscope. The output voltage thus obtained is shown in Fig. 16.

In the oscilloscope the variation of output voltage can be observed while the simulation is on. Likewise the variation of the duty cycle can be viewed through the oscilloscope 2 as shown in Fig. 17.

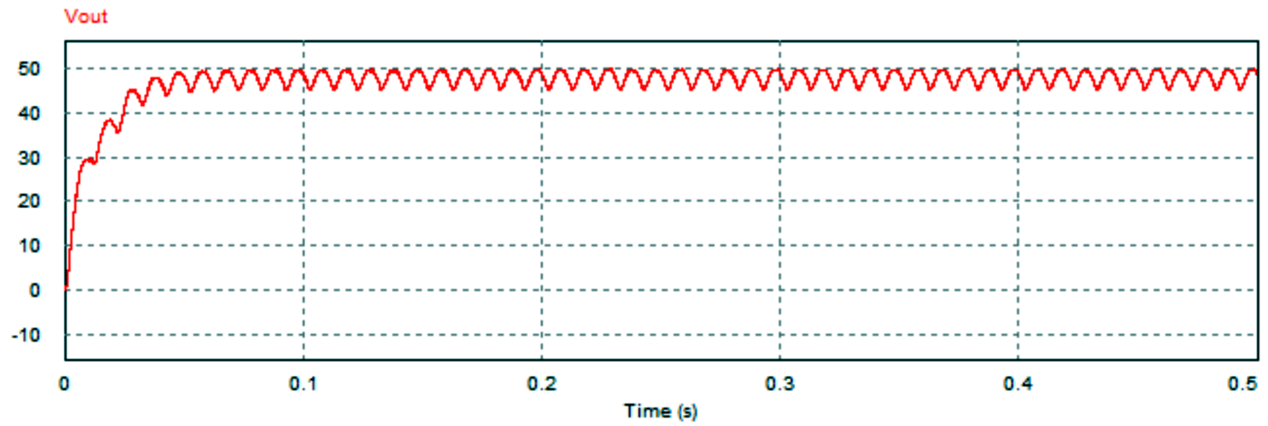

Fig. 10. Output voltage at an input of 250 V peak

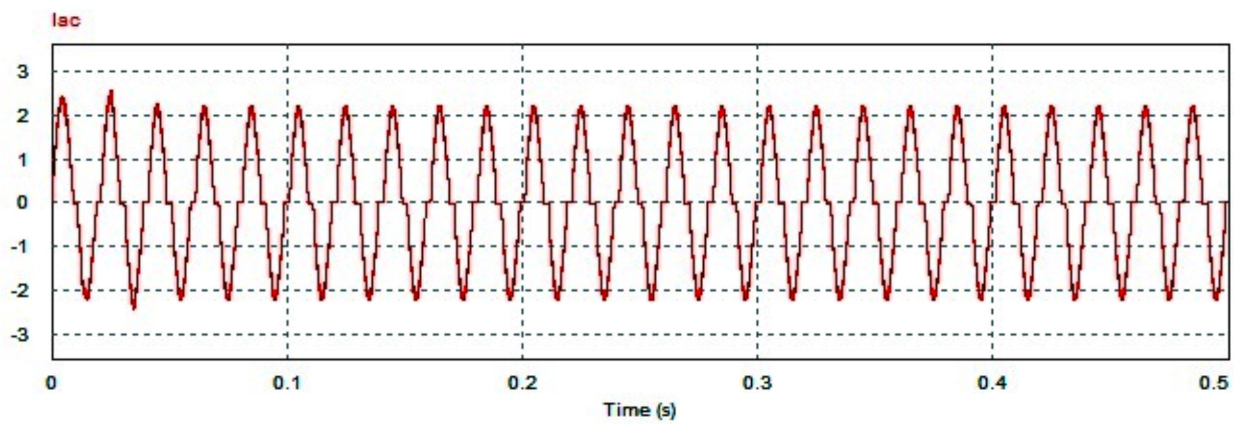

Fig. 11. Input current waveform

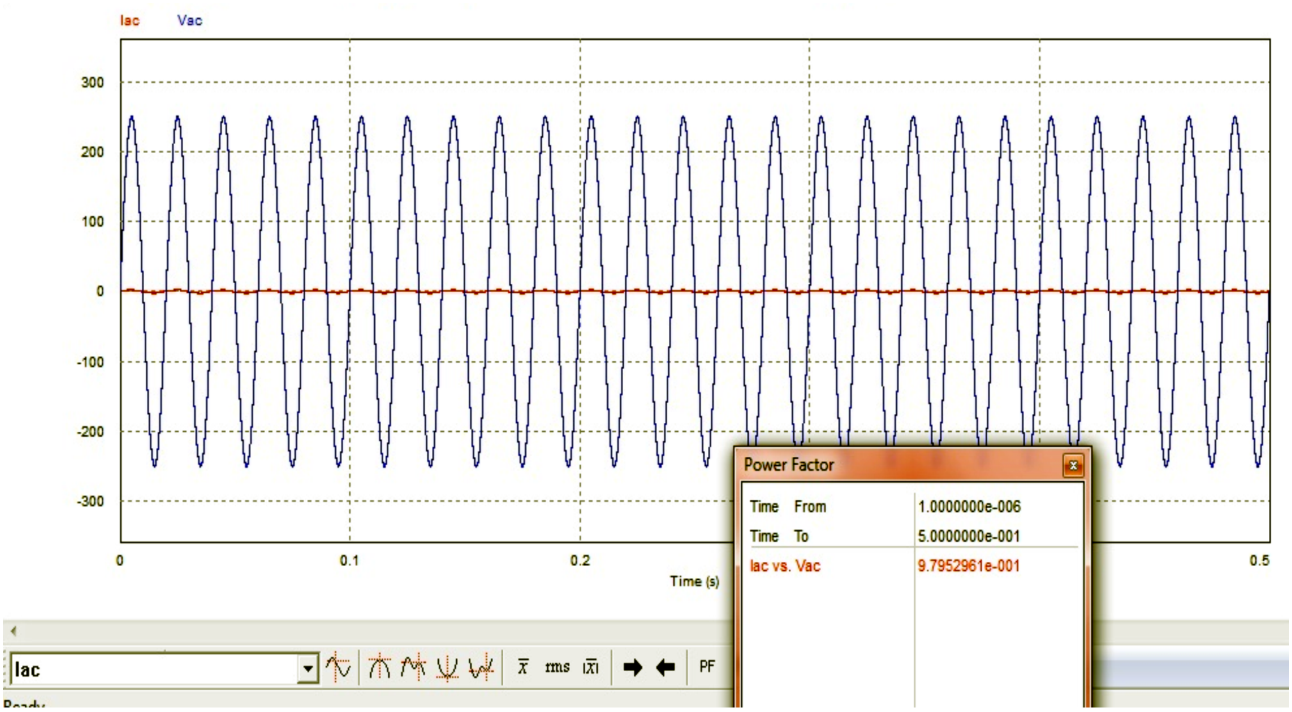

Fig. 12. Input voltage and current wave forms, showing power factor

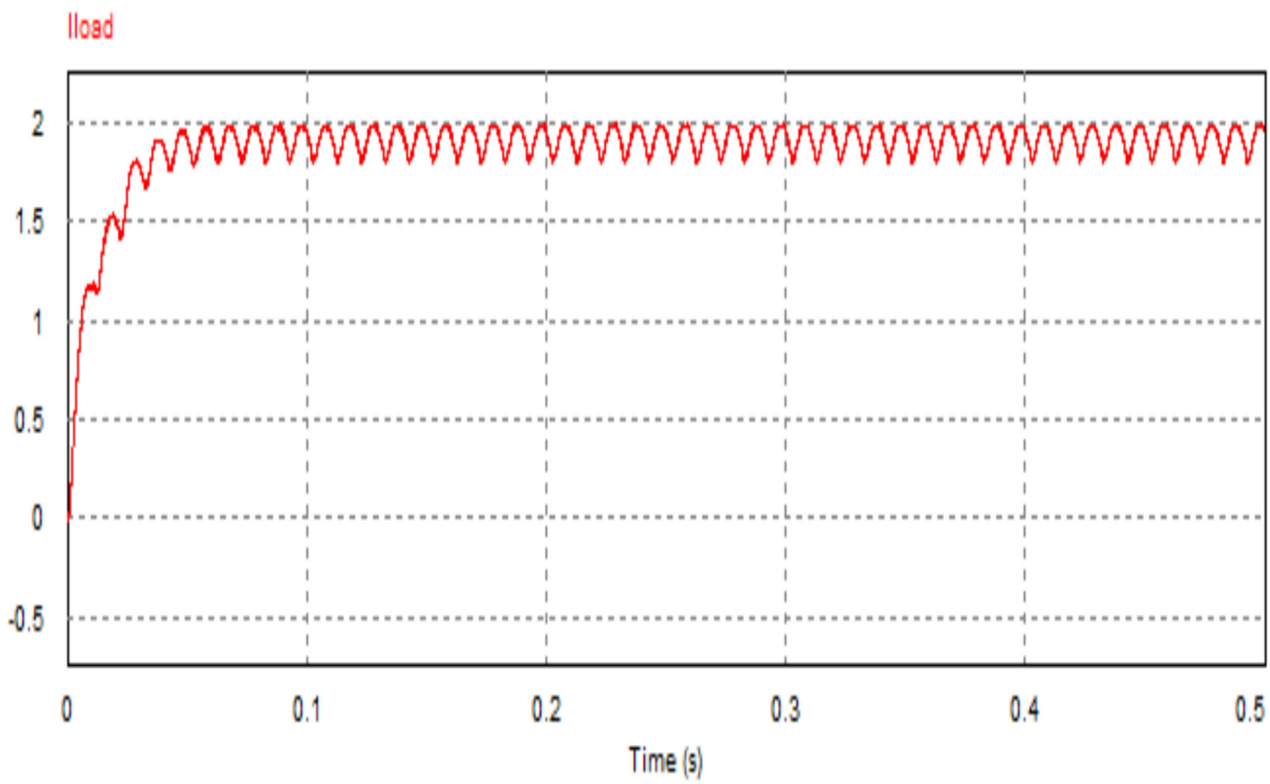

Fig. 13. Load current

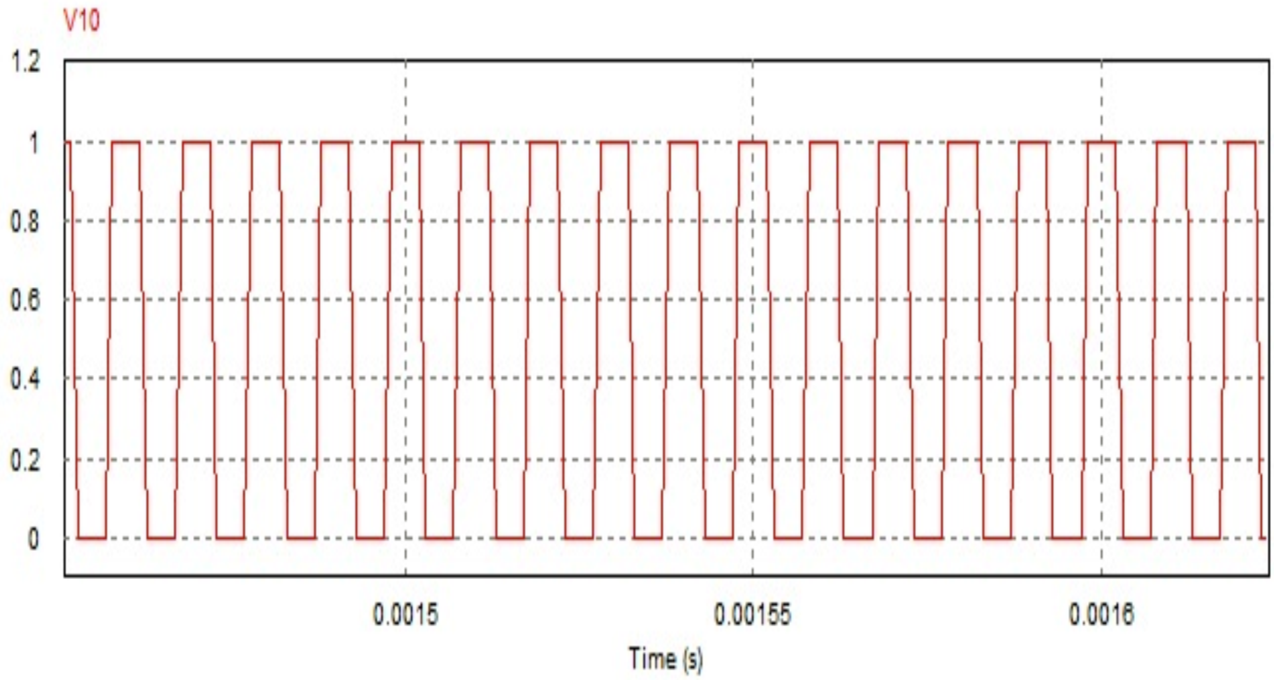

Fig. 14 Variation of duty cycle at the initial stage

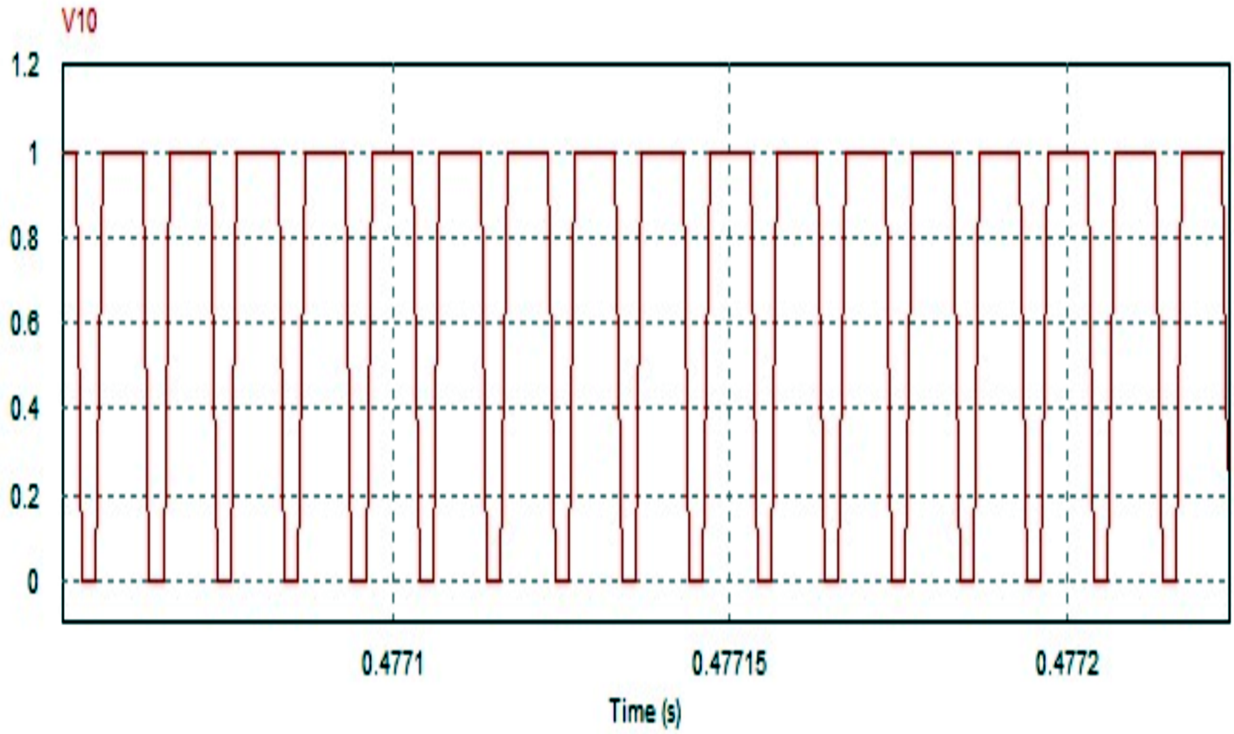

Fig. 15. Variation of duty cycle at the steady state stage

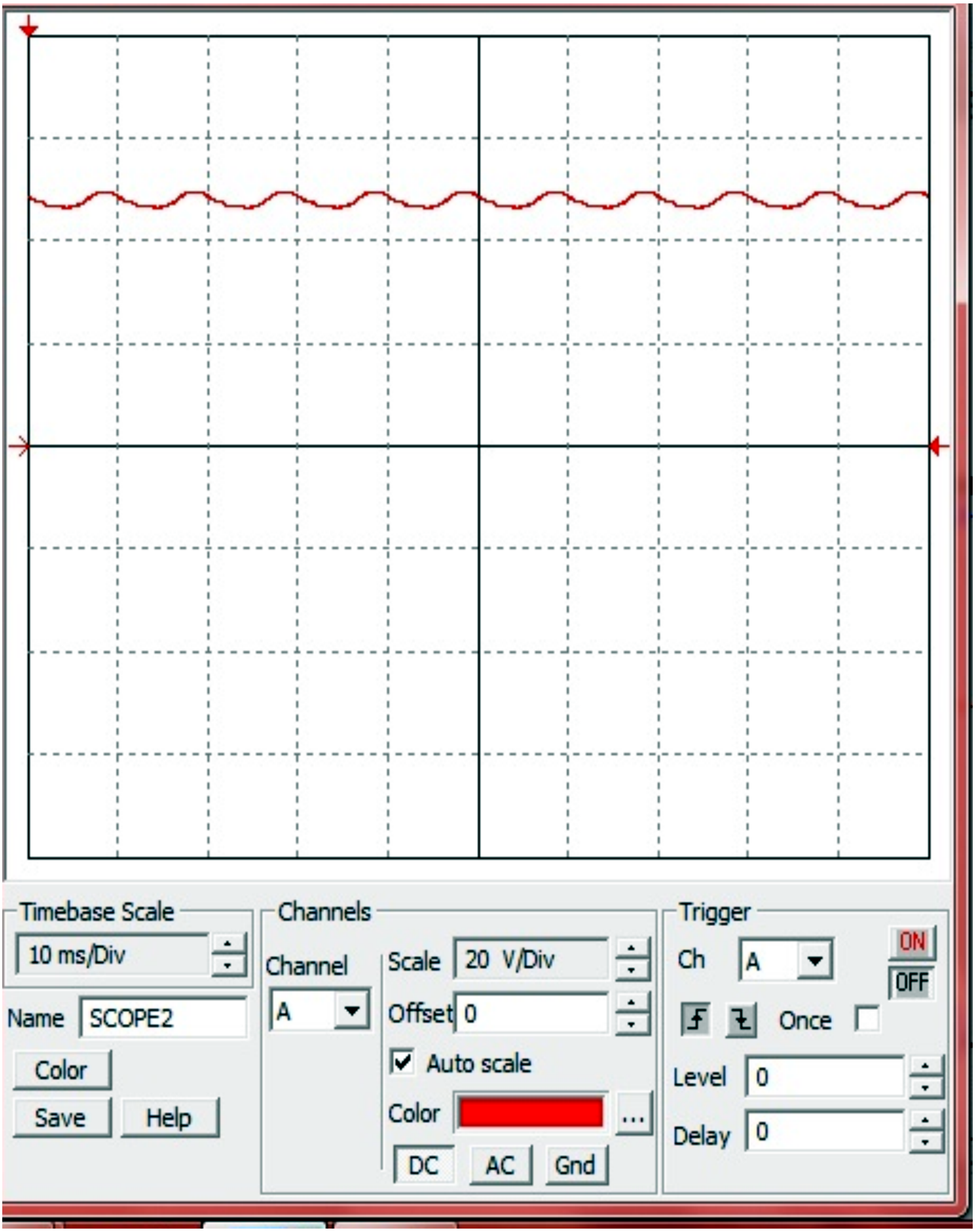

Fig. 16. The output voltage wave form on Oscilloscope

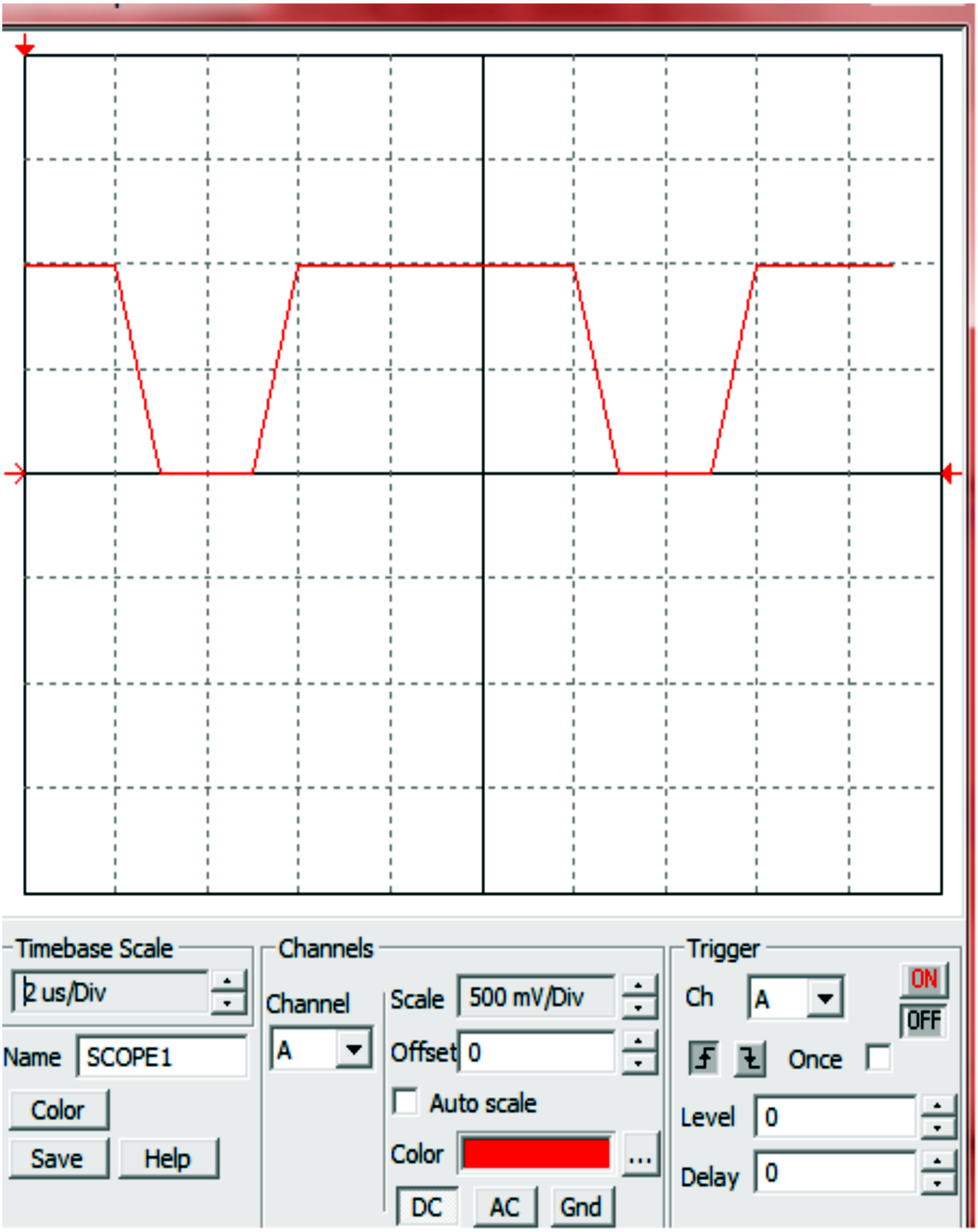

Fig. 17. Variation of duty cycle in oscilloscope

VI. CONCLUSION

Simulation of a High power factor Offline power supply for wide input ranges using IBFC is done in this paper. Both the Buck and Flyback converters are operated in discontinuous conduction mode. This circuit gives a good solution for low cost high power factor ac to dc converters with fast output regulation. The operation and advantages with this Single Stage Converter (SSC) is illustrated, showing how the control switch handles the lower rms current.

A Universal input of 90 - 250Vrms and 48V output and 100W output power operating at 100 KHz is designed. And simulation results show that maximum amount of active power is utilized since power factor is maintained high throughout the input voltage range. It is observed that the power factor is increasing with an increment of input voltage.

REFERENCES

[1] J. Marcos Alonso, Marco A. Dalla Costa, Carlos Ordiz, "Integrated Buck-Flyback Converter as a High-Power-Factor Off-Line Power Supply", *IEEE Transactions on industrial Electronics, vol.55, No.3, March 2008.*

[2] M. Madigan, R. Erickson, and E. Ismail, "Integrated high-quality rectifier regulators," *IEEE Trans. Ind. Electron.*, vol. 46, no. 4, pp. 749–758,Aug. 1999.

[3] M. Ferdowsi and A. Emadi, "Pulse regulation control technique for integrated high-quality rectifier-regulators," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 116–124, Feb. 2005.

[4] M.A. Dalla-Costa, J. M. Alonso, J. García, J. Cardesin, and M. Rico-Secades, "A novel low-cost electronic ballast to supply metal halide lamps," in *Conf. Rec. IAS Annu. Meeting, 2005, pp. 1198–1204.*

[5] M. Subba Rao "Design of Single-Phase DCM Integrated Buck-Flyback Converter for High Power Factor", *Int J Engg Techsci, Vol 2(2) 2011, 206-214.*

[6] David Gacio, J. Marcos Alonso, Antonio J. Calleja "A Universal-Input Single-Stage High-Power-Factor Power Supply for HB-LEDs Based on Integrated Buck–Flyback Converter" *IEEE Transactions on industrial Electronics*, vol. 58, No. 2, February 2011.

[7] Ned Mohan, Tore M. Undeland William P. Riobbins, *Power Electronics Converters Applications and Design, Wiley, India, 2009, chapter 10.*